★ MOTOROLA GRAPHICS CHIPSET, 1984

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The Motorola Raster Memory System

Making professional graphics affordable for the next generation of graphics systems

MOTOROLA INC.

Motorola Raster Memory System

LOW COST GRAPHICS FOR:

- *Personal Computers*
- *Work Stations*
- *Videotex Terminals*
- *Computer-Animated Graphics*
- *Word Processing*

WITH THESE FEATURES:

- *Multiple-processor Compatibility*
- *Multimode Operation*
- *32-Color Selectivity (From a Universe of 4096 Shades)*
- *Virtual Screen Accommodation*
- *Smooth Scrolling*
- *Memory Expandability*

2-CHIP SYSTEM

Today's electronics technology permits the generation of CRT-displayed graphics with all the fidelity of a first-quality color motion picture; but not at a price that is compatible with that of low and medium-priced micro-computerized equipment. Today, high quality graphics generation requires several printed circuit boards, densely packed with SSI/MSI integrated circuits, at a cost substantially above what is tolerable for microcomputers...even for some of the more sophisticated minis. Therefore, the overwhelming majority of graphics displays—for both business and entertainment—still suffer from the limited resolution and color selectivity associated with relatively crude arcade games.

But a significant breakthrough is in the offing. Using VLSI processing, Motorola has reduced the multi-board chip complement housing the complex circuitry for high-quality graphics to only two monolithic chips. At an anticipated combined price of less than $20.00 (in production quantities) this chip set portents a major upgrading of low and medium-priced computer graphics.

Though not yet in volume production, the design is sufficiently advanced to permit demonstration,* and to warrant consideration for the next generation of equipment design.

*It has recently been demonstrated at the Consumer Electronics Show, Las Vegas, Nevada, January 5-9, 1984.

MPU CHOICES

The Motorola RMS chip set actually consists of two chips which, under MPU control, convert a graphics program stored in memory to the complex video stream that produces high-quality information on the CRT. This two-chip video display generator set, supplemented by a microprocessor, memory to store the program data, and a small number (as little as three packages) of additional SSI/MSI interface chips, form a complete system. The interface chips act as "glue" for variations in overall hardware architecture.

Eventual display quality is controlled by the processing power of the MPU, the amount of available memory, the quality of the software and, of course, the capabilities of the video display generator. In this regard, the RMS chip set is designed to operate compatibly with three of Motorola's most advanced MPUs: the MC68000, 16/32-bit processor; the MC68008 which has all the processing power of the MC68000, but is designed with 8-bit data lines; the MC6809 with its 16-bit (rather than 32-bit) internal architecture and 8-bit data bus. This compatible MPU complement allows price/performance tradeoffs consistent with end-use requirements.

Going hand-in-hand with MPU selectivity is the ability of RMS to support memory capacity ranging from 16K to 1M Bytes. Again, end-use requirements determine the amount of memory, hence the cost, of the memory needs.

But the breakthrough comes in the myriad of functions crammed into the 2-chip graphics generator to provide the control for high-quality CRT graphics...resulting in a capability so pervasive that graphics quality is primarily dependent on the power of the MPU, the amount of memory available, and the sophistication of the software—*not by any limitations within the RMS system itself.*

- *Internal 96-character ROM*
- *8 reusable true objects*
- *Bit plane or list mode graphics*
- *Broad selection of attributes*
- *Kanji capability*
- *NTSC and PAL compatibility*

MULTI-MODE VIDEO

The RMS provides three unique sources of video generation: Bit plane graphics, list mode graphics, and true objects.

Bit plane displays can contain 4 colors in any resolution, and 16 colors in any horizontal resolution up to 320 pixels. They are most useful for creating complex graphics screens, interactively, under MPU control.

The RMS list mode is a character-oriented mode that supports up to 32 colors and four basic types of characters: alphanumerics, mosaics, fixed objects, and Dynamically Redefinable Characters (DRCs).

The major advantage of the list modes is their attributes. These include flash, double high/double wide characters, inverse video, priority, collision detection and reporting, etc.

True objects are small patterns in memory that the RMS can place on the screen, independent of the object's position in memory, simply by writing to X and Y position registers. The RMS provides eight true objects.

A major strength of the RMS is that the available modes of video operation are independent of the system configuration. Thus a high level of video performance is available over a wide range of system implementations.

CHOICE OF RESOLUTION

RMS operates with most popular CRTs. It will drive monitors with a 50 Hz field refresh rate, used in Europe, or with a 60 Hz rate popular in the U.S. And in either system you have a choice of resolutions up to 640 pixels per line, and up to 500 lines per screen (with 50 Hz refresh). For text reproduction, screen resolutions of either 32, 40, 64, or 80 characters per line are available...in full color. For graphics interpretation, choices of 256, 320, 512, or 640 pixels per line provide the needed definition to fit the application. All these choices are software selectable from internal horizontal and vertical resolution registers.

32 COLOR SELECTIVITY

RMS always operates in a full color mode. It can simultaneously display any 32 colors from its palette of 4096 colors. These are stored in a Color Mapping RAM (CMR) which is addressed, at pixel rate, as the video picture is generated. The system is extremely color selective, permitting the programmer to obtain adjacent pixels only slightly different in shade, as in flesh tones, or completely different in color, as in the reproduction of company logos.

- *Memory image larger than displayed screen*
- *Independent size and width registers to define the virtual screen*

VIRTUAL SCREEN ACCOM-MODATION

The user can construct a Virtual Screen much larger than the monitor's displayed screen using the RMS, then change the visible area by scrolling. The Virtual Screen can occupy as much as ½ Mbyte of memory, giving as much as:

15 displayed screens of 4-color bit plane (640 W x 210 H)

15 displayed screens of 16-color bit plane (320 W x 210 H)

174 displayed screens of 80-character x 25-character listmode (these will vary with the displayed screen's resolution)

The virtual screen can be almost any rectangle as large or larger than the displayed screen, varying in steps as small as one pixel or character row vertically, and 8 pixels or 2 characters horizontally. Three registers define the virtual screen's size, width, and start address.

- *Horizontal and Vertical Scroll*
- *Single Pixel Scrolling Resolution*
- *Minimal MPU Involvement*
- *Barrel Scroll or Edge Mask Effect*
- *Separate Position Registers for Objects*

SMOOTH SCROLLING

The RMS creates that perception of realistic screen motion by providing smooth scrolling in both the horizontal and vertical directions. The visible screen displayed in either bit plane or list mode can be moved within the larger virtual screen by one or more pixels at a time. This capability acknowledges the importance of processing time by requiring a minimum of actual MPU involvement. Since the hardware needed to display an image is controlled by only a few position registers, the entire background can be offset by a single line and/or pixel, or changed completely, in a matter of microseconds. Once the displayed screen is scrolled to the edge of the virtual screen, the programmer can select one of two boundary conditions: a barrel scroll (simply wrapping around to the opposite end of the virtual screen), or a single color edge mask that borders the virtual screen. Although controlled by a separate set of position registers, true objects can also be moved, pixel by pixel, providing lifelike animation.

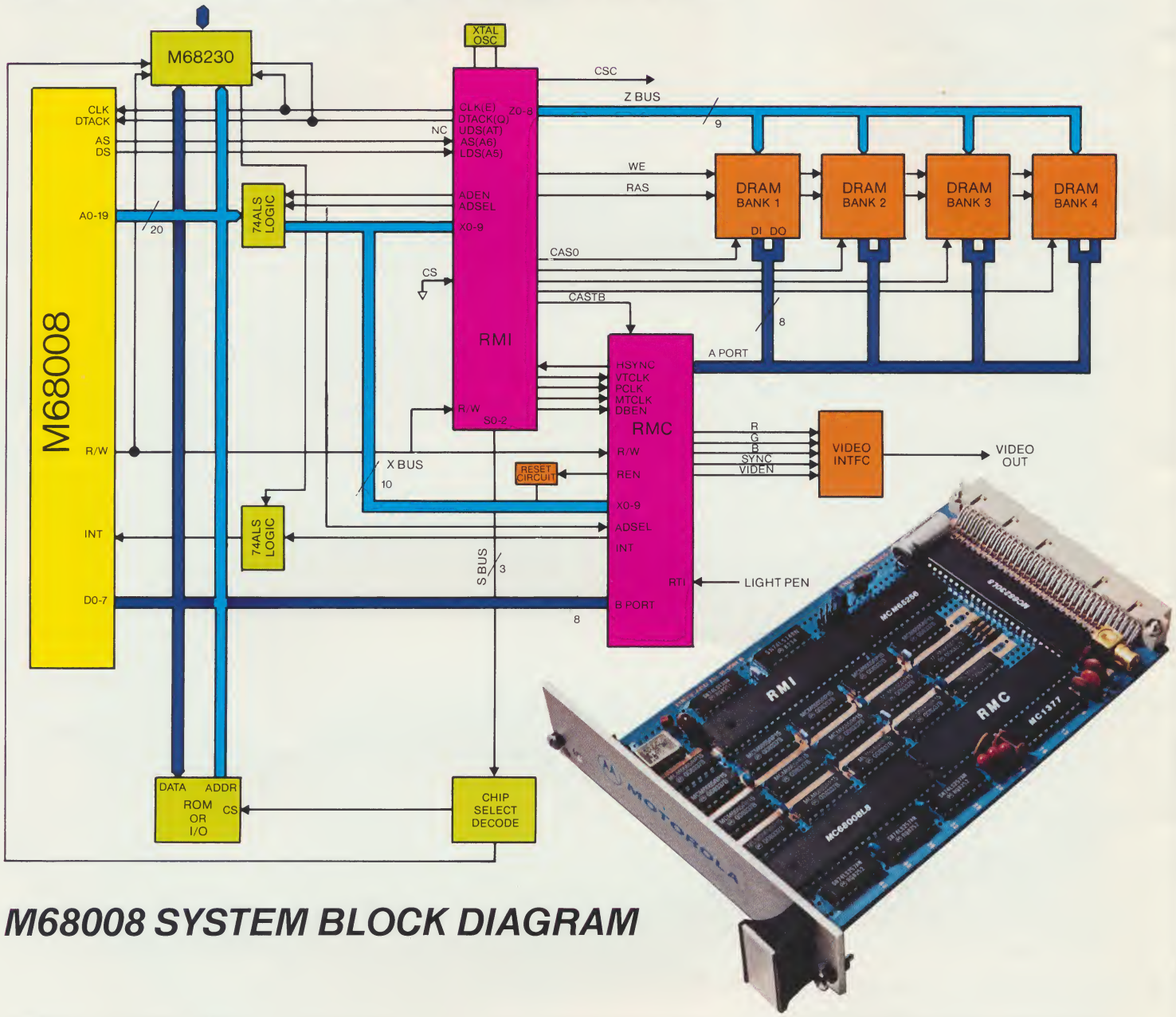
- *Supports 16KX1, 64KX1, 16KX4, and 256KX1 DRAMs*
- *Memory is shared by MPU and Display*
- *All memory timing, refresh, and buffering supported by RMS*
- *Supports 16K to 1M byte of DRAM directly*

MEMORY EXPANDABILITY

To provide maximum flexibility in system implementation, the RMS chip set operates in conjunction with dynamic RAM configurations from as small as 16K bytes to as large as 1M byte. It interfaces directly with several industry standard DRAMs; specifically, 16KX1, 64KX1, 16KX4, and 256KX1. Since memory is shared between the RMS and the MPU, the system designer need only concern himself with how much memory he would like; the RMS will take care of all the timing and refresh requirements. To minimize the total system RAM size, the MPU can access the shared dynamic RAM at the same time that it is being used for display purposes.

As little as one bank of memory is required to support the RMS system, but as system evolution or enhanced performance dictates, two or even four banks (equal length—byte-wide blocks) of memory can be configured to support higher level processors or more complex graphics. In general, the flexibility, expandability, and simplicity of memory interface to the RMS chip set is among its most significant features.

One Board Does It All



M68008 SYSTEM BLOCK DIAGRAM

RMS System The MPU-based System is quite straightforward and uses primarily VLSI devices. The major elements are the desired MPU, the RMS chip set, one to four banks of dynamic RAM, some "glue" and a video interface part. Additional RAM and I/O parts can be easily attached. The RMS itself consists of two parts: the Raster Memory Interface (RMI) and the Raster Memory Controller (RMC).

The RMI is a bipolar digital part built in Motorola's MOSAIC 1.5 process. This process provides the performance of Advanced Low-power Schottky (ALS) logic and also supplies the technology needed for high-density bipolar components. RMI provides the clock generation required for the entire system: the RMS, the MPU, and most peripherals. In addition, it provides DRAM timing, and passes address information between the MPU, the RMI and the RMC (via the X bus) as well as control information from the RMC to the RMI.

The RMC The RMC is a VLSI part fabricated in Motorola's HCMOS technology. The RMC uses the X bus to pass display addresses to the RMI. Once the RMI has addressed the DRAM, the data stored in the addressed locations is read by the RMC which, in turn, processes the data into video pixel information. Thus, the RMC is responsible for generating the sequence of memory addresses in which the video data is stored, and for converting this data into the video information passed on to the CRT.

The memory cycle in RMS allows nine chances to pass data on the X bus. Two of these are reserved for MPU address, two more are reserved for display addresses passed from RMC to RMI, and the remaining five cycles are used for control information.

Personal Computer Graphics System Comparisons

The following table compares the characteristics of the Motorola Raster Memory System (RMS) with those generally employed in today's high-, medium-, and low-end personal computer graphics equipment.

ATTRIBUTES	HIGH END	MID RANGE	LOW END	RMS
Resolution	640 x 200	320 x 210	320 x 210	640 x 500
Virtual Screen				√
Smooth Scroll Horiz.				√
Smooth Scroll Vert.				√
Color Palette*	16/16	16/16	16/4	4096/32
Screen Memory (max)	16K	16K	64K	1024K
Processor Memory Space	1024K	64K	64K	16,384K
80 Characters	√			√
DRCS**			√	√
Kanji				√
Objects			8	8
No. Of Memory Images			46	256
Color/Object			4	32
Overlay				√
NAPLPS Videotex	Fair	Fair	Fair	Excellent
Approx. IC Parts Count (in a typical system - less RAM)	130	45	40	14

*Palette: universe of colors available
**DRCS: Dynamically Redefinable Character Set

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Sep 84

"Graphics chip set paints a broad spectrum"

is the headline over the cover story of the January 26 issue of ELECTRONIC DESIGN. The article, featuring the Motorola Raster Memory System, and co-authored by Motorola engineers, is reprinted on the following pages for your information and convenience.

MOTOROLA INC.

BehindTheCover

As engineers well know, there are some expensive work stations with good graphics and many low-cost systems with limited graphics, but little in between.

In that large hole, a two-chip set has sprouted. The subject of our cover, it represents a low-cost—but high-resolution—solution to real-time graphics for engineering work stations. As Adrian Kuzdas, Motorola's systems engineering manager, puts it, "We saw an opportunity and started the development of silicon in 1982, with the goal of keeping the cost down yet providing at least 640 by 500 pixels with a choice of 4096 colors, object handling capability, and the ability to operate at video dot rates of up to 14.2 MHz."

To do that, though, required many tradeoffs, not only to define what features to put on the silicon, but also to determine the best processes and techniques with which to implement the functions. What resulted, according to Pat O'Malley, a principal staff engineer, is one chip implemented with 3-μm HCMOS; the other, with the company's low-power Schottky process. Together, both chips boast about 60,000 transistors.

But the technology story doesn't end there. The HCMOS part places a metal silicide coating on top of the polysilicon interconnections to reduce on-chip propagation delays, and the bipolar chip calls upon one of the most advanced oxide-isolated, ion-implantation processes (MOSAIC 1.5). CMOS provided the low power levels required of the controller chip—it is about five times as dense as the bipolar chip—and bipolar technology supplies the drive capability and speed needed to handle the external memory array and video dot speeds.

One of the hardest jobs in developing the chip set, according to Kuzdas, was the long-distance coordination needed to make sure that the bipolar and CMOS design teams—which were located in different cities—worked properly together. To visualize the chips' potential, the usual computer simulation was insufficient, so O'Malley guided the creation of a breadboard—15 large printed circuit boards containing over 1400 ICs.

On top of those, many breadboards had to be built to evaluate customers' requests for software development systems. Without those, O'Malley states, the design team would not have found some potential problems with the original circuit design.

Interestingly, after the first few problems were solved, all the others turned out to be idiosyncrasies of the breadboards—poor wrapped-wire interconnections, poor ground separations, and so on. But these problems helped the team avoid possible problem areas in designing the final silicon.

Design

A two-chip color video display generator creates a wide range of graphics. It works with three popular microprocessors and can be configured with a variety of dynamic RAMs.

Graphics chip set paints a broad spectrum

Spanning video graphics applications from complex personal computers and engineering work stations to simpler systems, a chip set that generates video displays gives designers a hardware tool for a full range of graphics performance. The pair produces text and graphical information for computer-aided design and word processing, as well as for education and entertainment.

The set operates with any of three popular microprocessors—the M6809E, M68008, and M68000. Moreover, it accommodates up to 1 Mbyte of industry-standard dynamic RAM. The Raster Memory System, or RMS, as it is known, is also highly programmable. A designer starts by defining a hardware system and then proceeds to choose the appropriate video mode. Once the hardware is selected, it varies little from one application to another. Improvements in performance result instead from the microprocessor employed, and amount of memory available, and the level of sophistication of the system software.

The RMS comprises the MC68486 Raster Memory Interface and the MC68487 Raster Memory Controller. The chip set operates with a variety of CRTs. In a low-end system, in which the horizontal resolution is between 32 and 40 characters/line, it can run a conventional television receiver. In more advanced systems, it can generate from 64 to 80 characters/line to fully take advantage of the higher resolution of color monitors.

The chip set generates both the PAL and NTSC video timing standards for a 50- or 60-Hz field-refresh-rate. The maximum vertical resolution for the former is 500 lines; for the latter, 400. Table 1 lists the range of vertical and horizontal combinations that are possible with the system.

The raster memory system always operates in color. Although it can generate 4096 hues, a programmer cannot use all of them at the same time. Generally, a set of 32 colors is selected from the total palette. A special memory, called a color mapping RAM (CMR) makes it possible to select colors without any restrictions. Among its many features,

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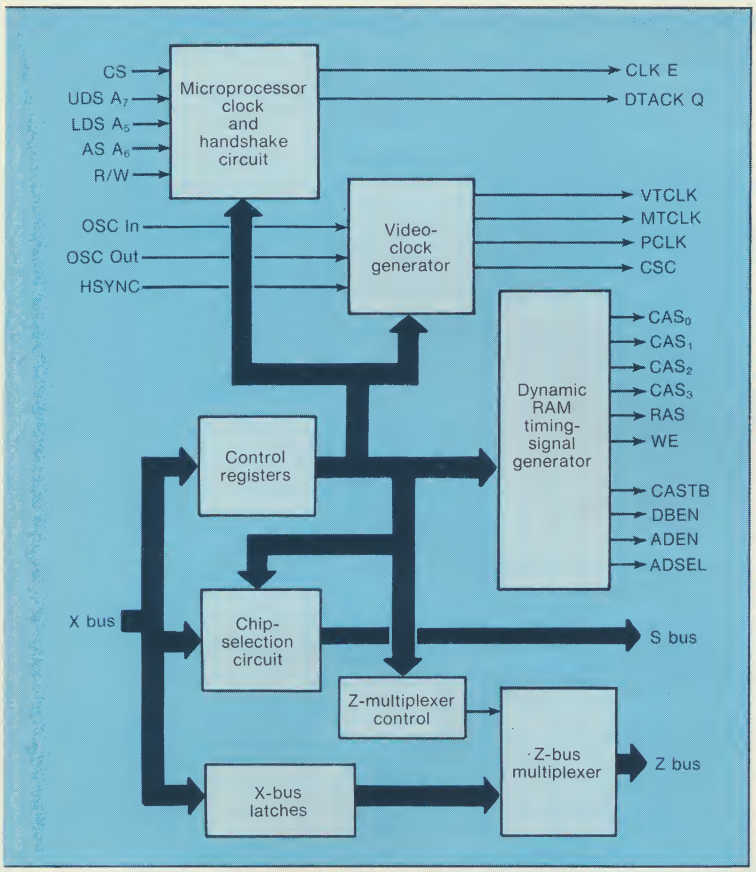
the RMS can be combined with another video source to create more complex images than the chip set can create alone. Among the sources that can be linked to the system are a video disk, broadcast video, or any other supply of compatible video—including a second RMS. A mechanism within the RMS allows it to be synchronized to other sources using a minimum of hardware. This ability allows RMS-generated images to overlay those from an external source.

No glue required

An important benefit of the approach is that the hardware required to build a microprocessor-based video system consists almost entirely of LSI devices.



1. Clock generation, dynamic RAM timing, address multiplexing, and device-selection decoding are some of the functions supplied by the raster memory interface chip. The high-speed bipolar device links external components to the raster memory system.

Very few SSI, or glue, chips are needed. The major elements of such a system are the microprocessor, the chip set, one to four banks of dynamic RAM, and a video interface. If necessary, a ROM and I/O chips can be easily added.

Several features are supplied to ease the designer's task. The master oscillator, for example, generates clock signals for the system, the microprocessor, and most of the peripherals. Chip-selection decoding is also simplified since the RMS can decode addresses other than its own. By adding a 3-to-8-line decoder, it is possible to generate chip-selection signals for the system and for seven other devices. What's more the RMS can deliver microprocessor handshaking signals for many of those peripherals in 68000-based configurations.

RAM requirements are simple to manage because the dynamic RAMs are truly a joint resource of both the microprocessor and the display-generator system. The latter serves as a dynamic RAM controller to make possible transparent refresh without additional components.

In the chips

Figure 1 shows the block diagram of the raster memory interface, a bipolar digital device fabricated with the MOSAIC 1.5 μm process. That technology combines the performance of advanced low-power Schottky with the circuit density needed for an LSI device. The chip generates the clock signals for the entire system, drives the microprocessor clocks, and supplies the dynamic timing and subcarrier signal for composite video. It also furnishes the microprocessor handshaking signals, such as DTACK, required by the 68000 family.

The raster memory interface is responsible for interfacing with the various dynamic RAMs that the system can employ. It multiplexes addresses from the raster memory controller and from the microprocessor into row and column addresses for the the dynamic memory. The Row Address Strobe and Column Address Strobe (RAS and CAS) timing signals are generated by the memory interface as well. No external buffers are needed, even with up to four banks of RAMs. The bipolar chip generates several types of memory cycles, depending on the amount of data that must be returned from a memory access. Page- and nibble-mode cycles are used to maximize the memory bandwidth, thus allowing for a high data throughput.

The raster memory controller, shown in Fig. 2, is a VLSI chip fabricated using Motorola's HCMOS process. It generates the addresses of the data that produces the video signal and processes data received from the dynamic RAM into video signals. All of the circuitry for generating the video timing

Table 1. RMS video-screen resolution combinations

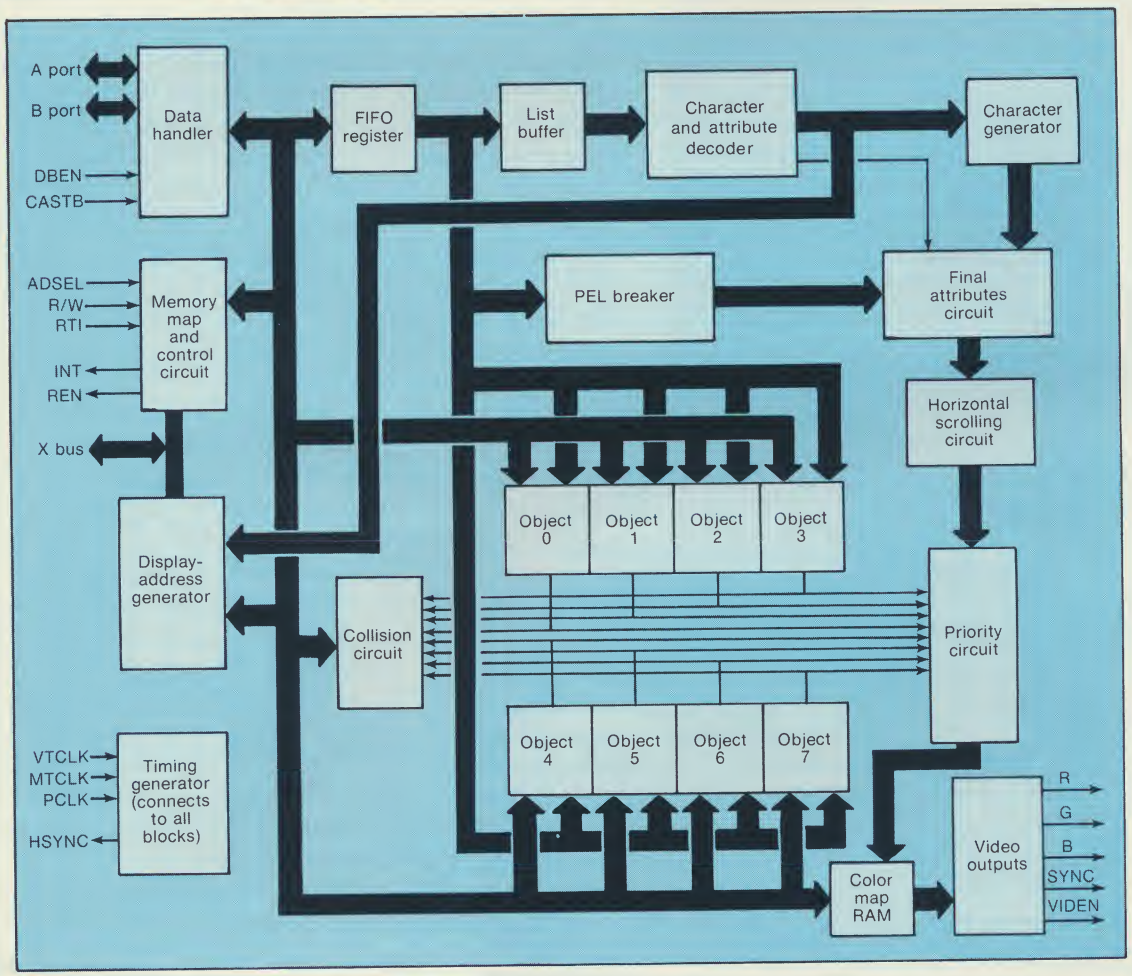
Vertical resolution (pixels)	Horizontal resolution (pixels)			
	256	320	512	640
192	None	None	Color limit	Color limit
200	None	None	Color limit	Color limit
210	None	None	Color limit	Color limit
240	50 Hz	50 Hz	50-Hz color limit	50-Hz color limit
250	50 Hz	50 Hz	50-Hz color limit	50-Hz color limit
384	Interlace	Interlace	Interlace color limit	Interlace color limit
400	Interlace	Interlace	Interlace color limit	Interlace color limit
420	Interlace	Interlace	Interlace color limit	Interlace color limit
480	50-Hz interlace	50-Hz interlace	50-Hz interlace color limit	50-Hz interlace color limit
500	50-Hz interlace	50-Hz interlace	50-Hz interlace color limit	50-Hz interlace color limit

signals is contained on the controller. The X bus delivers microprocessor address information to the chip, but it also passes video display addresses to the memory interface. The latter accesses the dynamic RAMs using the controller-supplied addresses, but the data is received at the controller.

The controller connects directly to the dynamic RAM and microprocessor buses. In many systems, it provides the separation between the buses. That separation is required because there are both microprocessor and display data present on the dynamic RAM bus at different times. Only microprocessor data, however, is permitted on the microprocessor data bus.

Down memory lane

Since the system works with several types of dynamic RAMs, a designer can select the memory based on the amount of storage needed, which can be as low as 16 kbytes or as high as 1 Mbyte. The dynamic RAMs that can be used are organized as 16k by 1, 16k by 4, 64k by 1, and 256k by 1. To ensure



2. The raster memory controller, an HCMOS device, generates all display addresses using data fetched from the system's dynamic RAM. From this data, the controller creates the bit-plane and list modes.

proper operation, the system requires a memory with a 150-ns access, which starts from the time a RAS is initiated.

The memory must be organized in byte-wide banks, and the system can work with one, two, or four such banks. With a single bank there will be a loss in performance because the data throughput rate will be lower. In addition, systems that use the 68000 must employ either two or four banks to properly support that microprocessor's 16-bit data bus.

The dynamic RAM is shared by the microprocessor and the video display, so it does not serve solely as a display buffer. Thus the microprocessor is guaranteed fast and regular accesses to the memory. In a form of time-division multiplexing, it is possible to execute programs stored in one section of the RAM while using another section as a display buffer.

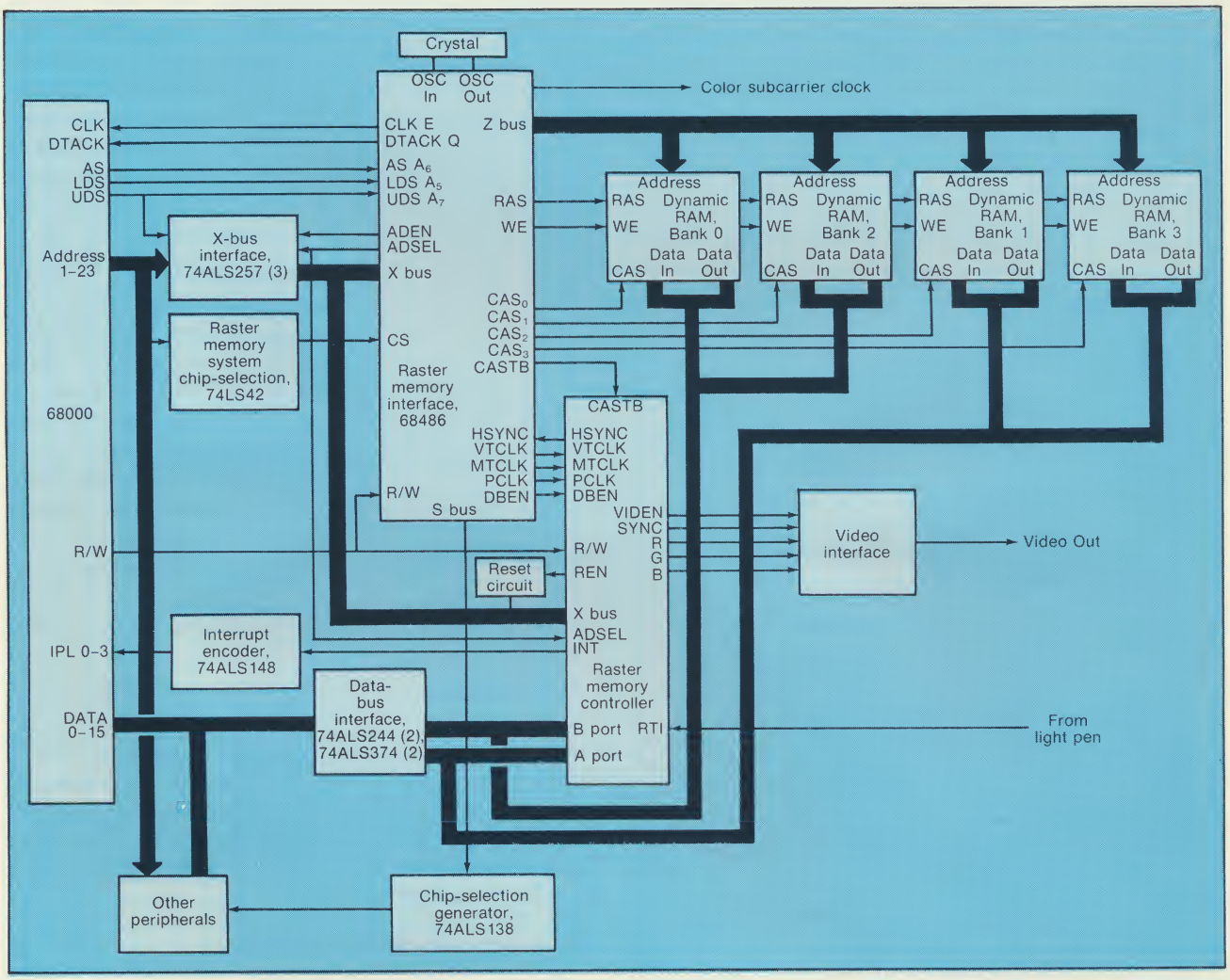
A basic memory cycle is approximately 1 μs in duration. During that time, both the microprocessor and the display process have an opportunity to access the RAM. Microprocessors such as the 6809E and 68008 are allowed to read or write one byte during the cycle. A 68000 can read or write either a byte or a 16-bit data word in that period.

A microprocessor's access to the memory takes about 300 ns, with the remainder of the time devoted to the display process. Since the video-display refresh usually proceeds sequentially through memory, the system makes extensive use of its page and nibble modes to obtain as much data as possible during the memory cycle.

Fetch and carry

The video process can fetch up to four bytes during its portion of the cycle. After raw data has been called from the RAM, it will be processed until it emerges as RGB (red, green, and blue) video signals suitable for the CRT.

Regardless of the microprocessor chosen, the



3. A personal engineering computer can be designed around a 16-bit 68000 microprocessor and the raster-memory chip set. The system handles up to 1 Mbyte of dynamic RAM directly and requires relatively few glue chips because most connections are handled by the interface chip.

basic structure of the video system remains the same. There will be some difference in the glue chips needed for each device.

Figure 3 illustrates a video-display system based on a 68000. The microprocessor's address bus, in conjunction with its upper data strobe and lower data strobe lines (UDS and LDS), provides a 16-Mbyte addressing range, but the system's entire RMS memory map occupies just 1 Mbyte. Normally, the four most significant bits of the microprocessor address are decoded to generate the chip selection signals for the 1-Mbyte memory. The remaining 19 lines, plus the UDS line, are connected to the system's X bus through three 74ALS257 multiplexers. That allows 20 bits of the microprocessor address to drive the chips in a time-division multiplexed scheme that employs only 10 pins.

In addition to its 16-bit data bus, the 68000 has a 24-bit address and a 32-bit internal architecture. The system works with the 8-MHz version of the 68000, for which it furnishes a 7.95-MHz clock. However, since the M68000 and the system interface asynchronously, it is possible to use faster versions of the microprocessor when higher performance is needed. In such systems, a designer must supply an external microprocessor clock. Accesses to the system or to the dynamic RAM, though, will occur at normal RMS speeds.

Table 2. Character attributes of the bit-plane mode

Attributes	Description
Flashing	The foreground part of a character alternates between the foreground and background color at a specifiable rate.
Underling	Alphanumeric characters are displayed with an underline.
CMR offset	Specifies the region within the color-map RAM from which the character's colors are selected.
Inverting	The foreground and background colors are reversed.
Double height	The character height is doubled.
Double width	The character width is doubled.
Color	Combined with the CMR offset to specify the CMR locations from which the foreground and background colors are displayed.
Color/ resolution	The character is displayed at half resolution with twice the number of colors.
Separation	Each of the blocks within a mosaic character is surrounded by the background color, thus separating the blocks displayed.
MOSAIC 4/6	Selects between 4 and 6 blocks within each mosaic character.
Collision enabling	Allows a collision between a fixed object and a true object to be reported to the microprocessor.
Priority	These bits assign a display priority to fixed objects so that a true object can pass in front of or behind a fixed object to give the illusion of depth.
Shading	Allows the color of a true object to change when it passes in front of a fixed object with its shading attribute set. It can be used to give the illusion of passing through shade.
Color collision	These bits allow parts of a fixed object to be affected by the collision, priority, and shading attributes while other parts remain unaffected.

Getting the picture

As the RMS generates a picture, data is pulled in from the memory and used to create pixels, which are 5-bit values in the system, but not associated with any color until they reach the final stages of processing. In those stages, the values are used to address the 32-word color mapping RAM. The contents of each 16-bit word define a color. Twelve of the bits—4 bits each for red, green, and blue can be programmed directly by the microprocessor.

The color mapping RAM is a powerful tool for controlling a video screen. In some applications, it creates many subtly different shades of the same color. In others, it generates a set of widely divergent colors.

Another important tool of the system is its so-called virtual screen, which comes into play when a picture will not fit on the screen without being compressed to the point that important details are lost. This is a common problem in spreadsheets, games, and certain CAD applications. In conventional video graphics systems, the programmer must store a large, complete picture in one section of memory. Subsets of the picture are then transferred to the screen-refresh buffer to create the desired display. That technique allows an operator to pan through the large picture, concentrating on individual sections. The problem is that each time the operator changes his point of view, large amounts of data must be moved from one part of the video memory to another. The time required for that move is dead time, and it quickly frustrates the operator.

The RMS eliminates that difficulty by supporting a virtual screen in hardware. A programmer defines its height and width using a few system control-registers. A number of screen sizes are possible, ranging from the same size as the display to tens of times larger in both the horizontal and the vertical dimensions.

Using a second set of registers, a programmer selects the size of the displayed screen. A third set of registers controls where the displayed screen starts inside the virtual screen. In that way, an operator can pan to various parts of the display without forcing the microprocessor to move any screen data. Changing an entire screen takes just a few milliseconds.

Fits many computers

The system has features that allow the same program to run on a variety of computers. For example, assume that a designer creates a diagram on his

engineering work station's high-resolution monitor. He or she then wants to display it on a home computer, which uses a low-resolution color television. If the virtual screen is defined identically for both computers, the same data base can be used. With the system, the resolution of the displayed screen can be tailored to that of the CRT, so that less of the original drawing can be viewed at one time on the home computer. All other display functions, however, remain the same.

Panning is linked with the ability to scroll the display screen. Scrolling controls in the system are more sophisticated than those available with other display-generator hardware. The RMS offers horizontal and vertical pixel-by-pixel scrolling for all types of screens. Smooth scrolling allows more accurate positioning of information and is easier for an operator to follow.

Two options are available when scrolling causes the display to reach the end of the virtual screen. The first, called wraparound scrolling, uses the virtual screen as a toroid. That is, if scrolling proceeds in one direction long enough, it eventually returns to the starting point. The second, treats the virtual screen as a rectangle. When the edge of the virtual screen is reached, the system automatically fills the off-screen locations with a constant.

The system has two user-selectable operating modes, bit-plane and list. In addition, true objects are always available. In the first mode, the system retrieves data from memory and converts it directly to pixel data. As each byte is received, it is broken down into several pixel-sized pieces. A programmer can select the number of bits used to define each pixel—with 1, 2 or 4 bits/pixel. That, in turn, determines the maximum number of colors that can be displayed simultaneously. For example, 1 bit/pixel permits two colors, 2 generates four colors, and 4

4. This scene, created in the bit-plane mode, illustrates the realism and high resolution possible with the raster memory system. The picture is formed by digitizing the Red, Green and Blue output signals from a color TV camera.

supports sixteen colors.

The bit-plane mode is very powerful because the data that define each pixel is completely independent of all other pixels. Thus a programmer is free to draw any shape without concern for interactions among pixels. Its disadvantage lies in the fact that it requires a large amount of data to draw a screen, which can have a negative impact on the application in terms of the memory requirements and execution time. Figure 4 illustrates a type of bit-plane display that the system can produce. The scene was created by digitizing the output of a color TV camera and converting the data into RMS-compatible bit-plane memory. The resolution is 256 by 200 pixels, using 4 bits/pixel.

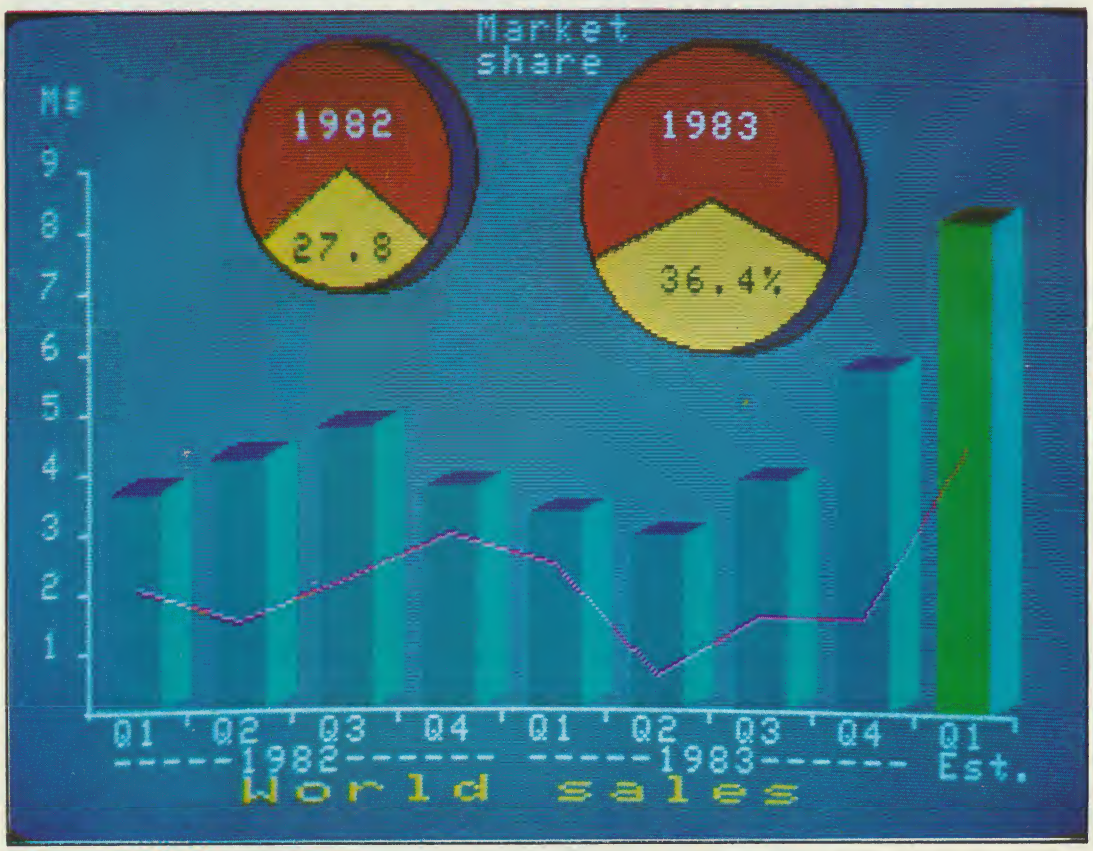
Making a list

In general, list mode has an advantage over the bit plane in that less memory is needed. Its disadvantages are that flexibility is lost due to interaction between pixels, and more planning is required to generate a drawing because memory is not contiguous. List mode can be thought of as an indirect mode. That is, the first data fetched from memory does not define the pixel pattern that will be ultimately displayed. Rather, it serves as an address to point the system towards a memory area where the pixel pattern is stored. This indirect technique works well when pixel patterns are well defined, such as with text.

Three different types of characters are supported in list mode: alphanumeric, mosaic, and redefinable. Alphanumeric-character patterns are stored in a ROM on the raster memory controller, which is invisible to the microprocessor. Patterns are automatically selected by the hardware when required. Since text is a major application of list mode, the pixel-pattern blocks that appear on the screen can be thought of as character locations. A character is either 8 or 16 pixels wide and user programmable. Also programmable is character height, with options of 8, 10, 12 and 16 scan lines available.

The major advantage of the list mode over the bit plane is the availability of a variety of attributes that can be specified for each character (Table 2). Clearly, the comprehensive list of attributes provides a substantial number of special features to be used to enhance the characters and make them more meaningful.

A sophisticated microcomputer such as a 68000-based personal engineering computer represents the upper limits of the chip-set's capabilities in a general-purpose application. The basic requirements of such an application are to maximize the



5. Multicolored comprehensive and detailed bar and pie charts are readily handled by the system.

throughput of the microprocessor and the system RAM. Thus the 16-bit 68000 is selected as the microprocessor. The system supports a full megabyte of RAM—four banks of 256 kbytes each—which should be adequate for the engineering machine. If additional memory is necessary, its address decoding, chip selections, and refresh circuitry must be provided with external components.

Size and speed

It is unlikely that the design will require either a faster version of the microprocessor or additional dynamic RAM. Such improvements are needed only in special applications having exceptionally large memory requirements or carrying out intense computations. Since the video-memory manipulation capabilities of the system substantially reduce the microprocessor's overhead tasks, there is little need for extreme processor speed or massive storage.

The block diagram of the personal engineering computer (Fig. 3, again) shows that relatively few glue chips are needed because the RMS provides microprocessor handshaking and chip selection for peripheral devices. The key handshaking signal is Data Transfer Acknowledge (DTACK). When it goes high, the 68000 knows that the device it is communicating with has either read the data it put on the bus for a write operation or has put data on the bus for the 68000 to read. It is the designer's choice to have the raster memory system generate DTACK for all or for some of the system peripherals. The only requirement is that the peripheral be fast enough to respond to DTACK within the time frame allotted by the system. Any device that does not use the handshaking signals must either inform the 68000 that it is a 6800 family member and intends to handshake in a synchronous manner or must furnish its own DTACK to the processor.

The remaining interface lines between the 68000 and the system are straightforward. If the microprocessor uses the system-generated clock, it must be connected from the memory interface chip. Likewise, Address Strobe (AS), Upper Data Strobe (UDS), Lower Data Strobe (LDS) and Read/Write (R/W) connect to the 68000 from the interface. The AS line is a handshaking signal that indicates to the system that the address on the processor bus is valid and that the processor is ready to initiate a machine cycle. UDS and LDS serve two functions: The processor uses them to indicate whether the current cycle involves the high-data byte, the low-data byte, or both, of a 16-bit transfer. The UDS and LDS bits are also used by the interface chip as part of the asynchronous interface with the 68000 to indicate that the current processor cycle has ended. R/W connects to both chips to indicate whether the current cycle is a read or write.

Connecting a dynamic RAM and microprocessor to the system is more difficult with the 68000 than with an 8-bit processor because the RAM and processor buses must be separated, except at specific times. The memory controller's two 8-bit ports need help to accomplish that separation, which comes in the form of four 74ALS logic devices: two 74ALS374 8-bit latches and two 74ALS244 8-bit buffers. The latches hold RAM data during a processor read-cycle and go into a three-state mode for the rest of the time. The buffers drive the processor during a write cycle and are otherwise in three-state mode.

The RMS can generate interrupts to the 68000. The interrupt (INT) line normally runs from the controller to the encoder chip whose outputs are connected to the 68000's interrupt inputs. That means that the system's interrupt priority level is selected in hardware.

Memory accesses from the 68000 to the system or to the dynamic RAM cannot occur at the maximum speed of the processor. The RMS adds two wait states (250 ns each) to every processor memory access. This is a restriction, but not severe enough to justify its elimination, which would require the use of expensive, high-speed memory components.

System operates synchronously

Another restriction on processor throughput results from the fact that the system operates synchronously to maintain a steady stream of video information to the screen, which in turn means that processor accesses are permitted only at specific times. Since the length of cycle closely matches with most 68000 memory fetches, the processor spends little or no time waiting for the bus. However, the processor will at times request data at an instant that the system is unable to provide it. In that case, the processor must wait in the same manner as it would when accessing a 6800 family peripheral, although not as long.

Figure 5 illustrates a detailed bar and pie chart in color. The pictorial block diagram was created at a resolution of 320 by 210 pixels and with 16 colors. This could be just a small part of a complete set of charts; scrolling would allow a user to view other parts throughout the virtual screen. It is possible to produce figures and charts with higher resolutions, 640 by 400 pixels. That would provide much greater detail, although the number of colors would be reduced to four.□

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